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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/517,705	03/02/2000	Chunlin Liang	042390.P5771D	4202

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Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard 7th Floor
Los Angeles, CA 90025

EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/517,705	LIANG ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,16-18,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 16-18, 20, 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 17 and 21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification never discloses the first metal gate electrode having a work function corresponding to the work function of N-type silicon is one of tantalum nitride and molybdenum nitride as claimed in claim 17.

The specification never discloses the first metal gate electrode having a Fermi level corresponding to the work function of P-type silicon is one of tantalum and molybdenum silicide as claimed in claim 21.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 18 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Kuroi et al.

In regards to claim 1, Kuroi et al. show all the elements of the claimed invention in fig. 9. It is a circuit device, comprising: a first transistor (NMOS) [42] including a first metal gate electrode (n-type titanium silicide film [41] which formed above layer [29])

over a first gate dielectric [4] on a first area [24] of a semiconductor substrate [1], the first metal gate electrode comprising a first metal layer (n-type titanium silicide film [41] which formed above layer [29]) having a work function corresponding to the work function of the N-type silicon; and a second transistor (PMOS) [43] complementary to the first transistor including a second metal gate electrode (p-type titanium silicide film [41] which formed above layer [31]) over a second gate dielectric [4] on a second different area [25] of a semiconductor substrate [1], the second metal gate electrode comprising a second metal layer (p-type titanium silicide film [41] which formed above layer [31]), the second metal layer having a work function corresponding to the work function of the P-type silicon; and wherein the first metal gate electrode and the second metal gate electrode are each separately disposed in respective ones of the first area [24] and the second area [25] of the semiconductor substrate, and wherein the first metal layer and second metal layer comprise the same type of metal (titanium).

In regards to claim 18, Kuroi et al. show all the elements of the claimed invention in figs. 9 and 10A to 10D. It is a circuit device, comprising: a first transistor (PMOS) [43] including a first gate electrode (p-type titanium silicide film [41] which formed above layer [31]) over a first gate dielectric [4] on a first area [25] of a semiconductor substrate [1], the first gate electrode comprising a first metal layer (p-type titanium silicide film [41] which formed above layer [31]) having a Fermi level corresponding to the work function of the P-type silicon; and a second transistor (NMOS) [42] complementary to the first transistor including a second metal gate electrode (n-type titanium silicide film [41] which formed above layer [29]) over a second gate dielectric [4] on a second different

area [24] of a semiconductor substrate [1], the second gate electrode comprising a second metal layer (n-type titanium silicide film [41] which formed above layer [29]) having a Fermi level corresponding to a work function of the N-type silicon; and wherein the first metal gate electrode and the second metal gate electrode are each separately disposed in respective ones of the first area [25] and the second area [24] of the semiconductor substrate, and wherein the first metal layer and second metal layer are formed from a same initial metal layer (titanium film [44] of fig. 10B).

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 16, 17 are clear and definite, and 20, 21 insofar, as in compliance with 35 USC 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroi et al.

In regards to claims 16, 20, Kuroi et al. differ from the claimed invention by not showing the first gate dielectric is silicon dioxide. It would have been obvious to one of ordinary skill in the art to have silicon dioxide as the first gate dielectric because it is a conventional gate dielectric material.

In regards to claims 17, Kuroi et al. differ from the claimed invention by not showing the first metal gate electrode is one of tantalum and molybdenum silicide. It would have been obvious for the first metal gate electrode is one of tantalum and molybdenum silicide since it has been held to be within the general skill of a worker in the art to select

a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

In regards to claim 21, Kuroi et al. differ from the claimed invention by not showing the first gate electrode is one of tantalum nitride and molybdenum nitride. It would have been obvious for the first gate electrode is one of tantalum nitride and molybdenum nitride since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

6. Applicant's arguments filed 2/24/04 have been fully considered but they are not persuasive.

It is urged, in page 4 of the remarks, that Kuroi et al. never teach a first gate having a first metal layer that has a work function or Fermi level corresponding to the work function of an N-type silicon and a second gate electrode comprising a second metal layer having the work function or Fermi level corresponding to a work function of a P-type silicon. Although the conductivity type of the N-type and P-type gate electrodes is derived from the conductivity type of a polycrystalline silicon film 29 and 31, the N-type and P-type gate electrodes contain a metal element (titanium). Therefore, the n-type titanium silicide film [41] and the p-type titanium silicide film [41] are considered as metal layers. The n-type titanium silicide film [41] (the first metal layer) which formed above layer [29] has a work function or Fermi level corresponding to the work function of an N-type silicon, and the p-type titanium silicide film [41] (the second metal layer) which formed above layer [31] having the work function or Fermi level corresponding to

a work function of a P-type silicon. Kuroi et al. teach each of the elements of claims 1 and 18. Claims 16, 17, 20 and 21 are still obvious over Kuroi et al. because Kuroi et al. disclose metal layers in a first and second gate electrode that have N-type and P-type Fermi levels or work functions.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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May 5, 2004

Steven Loke
Primary Examiner